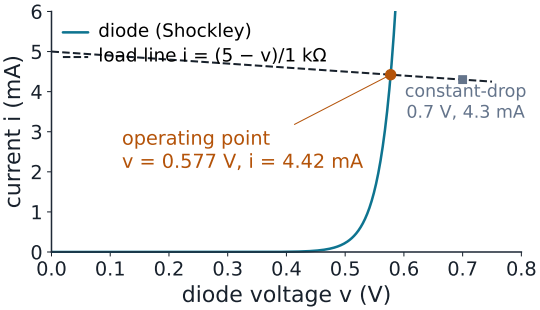
Electronics I

Curated undergraduate study track (not accredited, no external exam). Original explanations and practice only, following the reviewed course handout.

The devices take the stage

- Wave 1 and EE04 built the circuits; now the components themselves are the subject.
- **Modelling**: the simplest device model that answers the question - and a check for every assumption.

The load line meets the diode curve

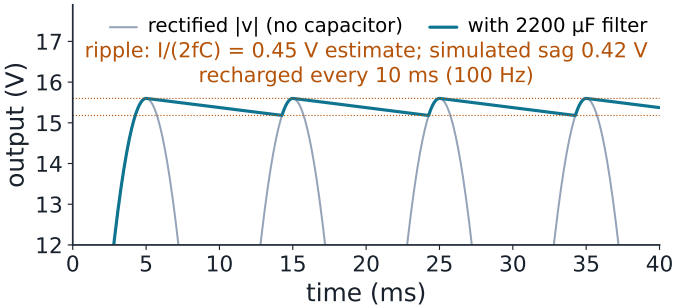


The Shockley curve is a near-vertical wall; the straight load line (5 - v)/1 kOhm fixes the current at 4.42 mA with v_D = 0.577 V, beside the constant-drop 4.3 mA.

The model ladder, three ways on one loop

1. **Ideal** 5 V source, diode, 1 k: 5 mA - the crudest bound.
2. **Constant-drop** (5 - 0.7)/1000 = 4.3 mA; bisection on the Shockley law gives 0.5775 V, 4.42 mA - within 2.8%.
3. **Dynamic** r_d = 26 mV/4.42 mA = 5.9 ohm: a 0.1 V wiggle drives 99.4 uA, 0.6% from the resistor-only 100 uA.

Rectifiers and dc supplies: the bridge and its ripple



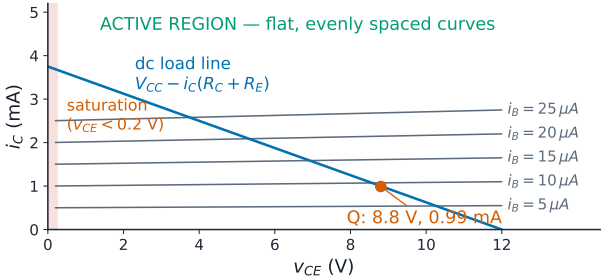
Full-wave rectified 15.6 V peaks with a 2200 uF filter at 100 mA: the output sags by 0.455 V between recharges every 10 ms.

A zener regulator, designed at both extremes

1. **Full load** R <= (12 - 5.1)/(10m + 2m) = 575 ohm -> pick 560; the zener keeps its 2 mA minimum.
2. **No load** I_Z = 6.9/560 = 12.3 mA: P_Z = 63 mW, resistor 85 mW worst case.
3. **Supply** 12 V RMS secondary: peak 12*sqrt(2) - 1.4 = 15.6 V, **ripple** 0.1/(100 x 2200u) = 0.455 V - 2.9% of peak.

BJT biasing: the Q-point on the output plane

Divider bias on the output plane: the Q-point and its check

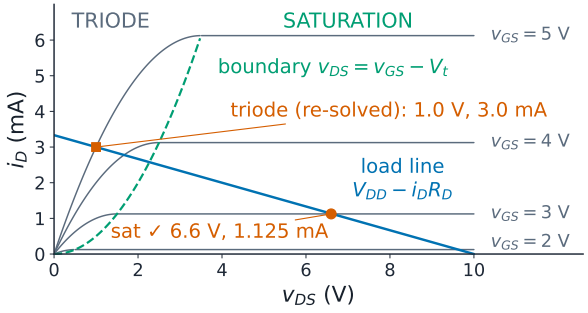


BJT output characteristics with the 12 V dc load line (R_C + R_E = 3.2 kOhm): the divider-bias Q-point sits on it at 0.99 mA, 8.8 V - well inside the **active region**.

Divider bias, exact - and the beta shield

1. **Exact** V_B = 1.8 V, R_B = 10.2 k: I_B = 1.1/(10.2k + 101k) = 9.9 uA -> I_C = 0.99 mA, V_CE = 8.8 V - active.
2. **Beta x2** beta 200: I_C = 1.04 mA - a 5% move; with R_E = 0 the active formula doubles, and saturation fails it.
3. **Errors** The quick 1.1 mA estimate was 11% high - base current loading the divider; both error sources now carry numbers.

MOSFET biasing: the boundary parabola is the region test



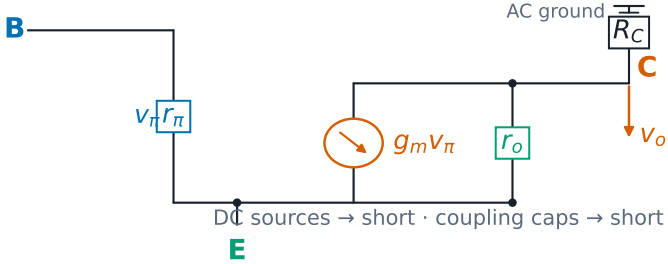
MOSFET i_D-v_DS curves for gates 2-5 V with the boundary parabola v_DS = v_GS - V_t: the 3 V gate sits in saturation at 6.6 V, the 5 V gate is caught and re-solved in triode at 1.0 V, 3.0 mA.

Assume saturation - and survive the check

1. **Stands** Gate 3 V: I_D = 0.5 x 1.5^2 = 1.125 mA, V_DS = 6.6 V >= 1.5 - saturation confirmed.
2. **Fails** Gate 5 V: saturation wants V_DS = -8.4 V - impossible; the resistor cannot drop 18 V from a 10 V rail.
3. **Triode** Load line + triode quadratic: v_DS = 1.00 V, i_D = 3.00 mA; the triode equation returns 3.0 mA - consistent.

Small-signal amplifiers: the hybrid-pi circuit

The hybrid-π model of the common-emitter stage



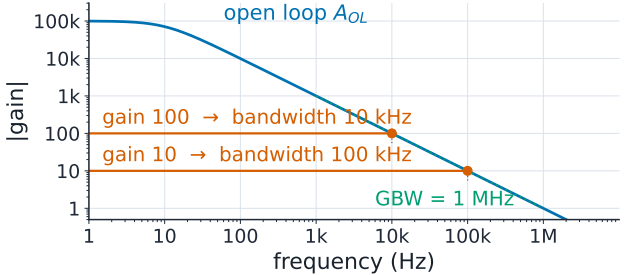
r_pi across base-emitter with v_pi, the controlled source g_m v_pi from collector to emitter, r_o in the collector leg and R_C to AC ground - every **small-signal** question answered by one circuit.

Gain, degeneration and the gm ledger

1. **Stage** I_C = 0.99 mA: g_m = 38.1 mS, r_pi = 2.6 k; with r_o = 50 k, A_v = -38.1m x 2.11k = -80 (r_o free: -84).
2. **Degen** -84/(1 + 38.1) = -2.14 against -R_C/R_E = -2.2 - within 2.4% because g_m R_E » 1.
3. **Compare MOSFET** at 1.125 mA: g_m = 1.5 mS, CS gain -4.5; the BJT 43.3 mS is 29x - transconductance for input resistance.

Op-amp feedback circuits: the gain-bandwidth hyperbola

Closed-loop gain buys bandwidth along the open-loop curve

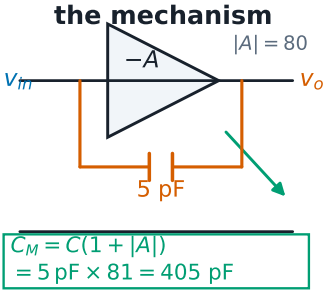


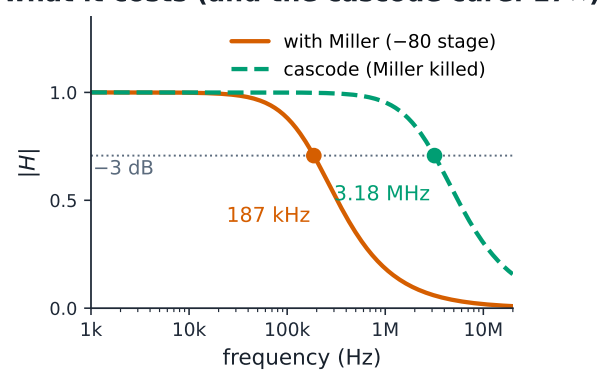
Open-loop response falling 20 dB/decade through the 1 MHz product; closed-loop lines at 100x and 10x meet it at 10 kHz and 100 kHz.

How wrong are the golden rules?

1. **Fresh chip** Closed-loop 100, A_OL = 1e5: A_CL = $100/(1 + 1/1000) = 99.90$ - a 0.1% error.
2. **Tired chip** Where A_OL has fallen to 1e3: A_CL = 90.9 - a 9.1% error.
3. **Corner** At 10 kHz a 1 MHz op-amp has A_OL = 100 = the closed-loop gain: **loop gain** 1 - the -3 dB corner itself.

Frequency response of amplifiers: Miller and the cure





5 pF across a gain of −80 acts as 405 pF; a cascode moves the corner to 3.18

The full band-pass, both corners

1. **Low** Coupling sees R_B || r_pi = 2.08 k: 10 uF gives f_L = 1/(2pi x 2.08k x 10u) = 7.7 Hz.
2. **High** Miller 5 pF x 81 = 405 pF + 20 pF stray: f_H = 1/(2pi x 2k x 425p) = 187 kHz.
3. **Both ends** Cascode: 25 pF -> 3.18 MHz (17x). Two cascaded stages: 187 x sqrt(2^0.5 - 1) = 120 kHz.

Check yourself

- Diode: the 5 V / 1 k loop with the **constant-drop model** reads? (4.3 mA.)
- **MOSFET**: the gate at 5 V lands the device in which region? (Triode.)
- Miller: 5 pF across a -80 stage appears at the input as? (405 pF.)